

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claim 1 (Withdrawn) A photolithographic device comprising:

a substrate; and

a pattern layer formed on said substrate including pattern features, said pattern layer having radiant energy transparent portions and radiant energy blocking portions, wherein said pattern features produce a varying overlay when exposed to radiation during a photolithography process.

Claim 2 (Withdrawn) The photolithographic device of Claim 1 wherein said varying overlay is produced by pattern features having a varying feature alignment.

Claim 3 (Withdrawn) The photolithography device of Claim 2 wherein said varying feature alignment comprises said pattern features misaligned in incremental degrees from a target feature alignment.

Claim 4 (Withdrawn) The photolithographic device of Claim 1 wherein said varying overlay is produced by said pattern features having a varying image size.

Claim 5 (Withdrawn) The photolithographic device of Claim 4 wherein said varying image size is produced by printing said pattern features having an image size in increasing and decreasing increments from a target dimension.

Claim 6 (Withdrawn) The photolithography device of Claim 1 wherein said varying overlay is produced by pattern features having a varying feature alignment and varying image size.

Claim 7 (Withdrawn) The photolithography device of Claim 6 wherein said pattern layer comprises a grid of said pattern features having said varying feature alignment and said varying image size, wherein said varying feature alignment comprises incrementally misaligned features from a target feature alignment; and said varying image size comprises incremental image size variations from a target image dimension.

Claim 8 (Withdrawn) The photolithographic device of Claim 1 wherein said pattern layer comprises chromium, chrome oxide, or chromium nitride.

Claim 9 (Currently Amended) A method for determining an optimum photolithography process window comprising:

exposing a portion of a single wafer to a pattern of a reticle, said pattern having pattern features producing varying overlay conditions, wherein each of said varying overlay conditions has an a different overlay tolerance contributed by both varying image size and pattern feature alignment built into a reticle design;

stepping said reticle across ~~[[a]]~~ one or more remaining portion portions of said single wafer, where each step exposes an other region of said wafer to said reticle pattern features producing said varying overlay conditions;

producing test structures from said varying overlay conditions;

and testing said test structures to determine said optimum photolithography process window.

Claim 10 (Original) The method according to Claim 9 wherein said pattern features further comprise a varying feature alignment and said each of said varying overlay conditions further comprises a feature alignment.

Claim 11 (Original) The method according to Claim 10 wherein said varying feature alignment further comprises said pattern features misaligned in incremental degrees from a target feature alignment.

Claim 12 (Original) The method according to Claim 9 wherein said pattern features further comprise a varying image size, wherein said each overlay condition further comprises an image size.

Claim 13 (Original) The method according to Claim 12 wherein said varying image size further comprises said pattern features dimensioned in increasing and decreasing increments from a target dimension.

Claim 14 (Currently Amended) A method for determining an optimum photolithography process window comprising:

exposing a single chip in a wafer to a pattern of a reticle, said pattern having pattern features capable of producing varying overlay conditions, wherein each overlay condition of said varying overlay conditions has an a different overlay tolerance contributed by both varying image size and pattern feature alignment built into a reticle design;

producing test structures from said multiple overlay conditions at said single chip; and

testing said test structures, wherein an optimum photolithography process window is determined from exposing a single chip on said wafer.

Claims 15 – 16 (Canceled).

Claim 17 (Withdrawn) A test wafer comprising:

a plurality of test regions; and

a plurality of test structures within each of said plurality of test regions, each of said plurality of test structures having a different alignment between a chain feature and a line feature within each of said test structures, said chain feature and said line feature each in contact with at least one test pad, wherein a total number of test pads within each of said plurality of said test regions is equal to:

a first number of test structures formed by a first photolithography condition multiplied by a first number of test pads required to measure each of said first number of test structures formed by said first photolithography condition; and

one or more other test structures formed by one or more other photolithography conditions multiplied by one or more other number of test pads required to measure each of said one or more other test structures formed by said one or more other photolithography conditions, wherein said first photolithography condition comprises a first alignment between said chain and line feature, and said one or more other photolithography conditions comprises another alignment between said chain and line feature.

Claim 18 (Withdrawn) The test wafer of Claim 17 wherein said total number of test pads within each of said plurality of said test regions is equal to:

$$[(N \text{ condition}) \times (\# \text{ test pads for } N \text{ condition})] + [(N' \text{ condition}) \times (\# \text{ test pads for } N' \text{ condition})],$$

wherein N condition is a first alignment between said chain and said line feature, N' condition is another alignment between said chain and said line feature, # test pads for N condition equals a number of test pads to test said N condition and # of test pads of N' condition equals a number of test pads to test said N' condition.

Claim 19 (Withdrawn) The test wafer of Claim 18 wherein said line feature and said chain feature of said plurality of test structures further comprise a different image size

and wherein N condition further comprises a first image size and N' condition further comprises another image size.

Claim 20 (Withdrawn) The test wafer of Claim 19 wherein interaction between said line feature and chain feature is determined from electrical measurements from said plurality of test pads.

Claim 21 (Withdrawn) A test wafer comprising:

a plurality of test regions; and

a plurality of test structures within each of said plurality of test regions, each of said plurality of test structures having a different alignment between a chain feature and a line feature within each of said test structures, said chain feature and said line feature each in contact with at least one test pad, wherein a total number of test pads within each of said plurality of said test regions is equal to:

a first number of test structures formed by a first photolithography condition multiplied by a first number of test pads required to measure each of said first number of test structures formed by said first photolithography condition; and

one or more other test structures formed by one or more other photolithography conditions multiplied by one or more other number of test pads required to measure each of said one or more other test structures formed by said one or more other photolithography conditions, wherein said first photolithography condition comprises a first image size of said chain and line feature, and said one or more other photolithography conditions comprises another image size of said chain and line feature.

Claim 22 (New) The method according to Claim 9, wherein said optimum photolithography process window takes into account regionality effects of the single wafer.

Claim 23 (New) The method according to Claim 14, further comprising stepping said reticle across one or more single chip portions of said single wafer, where each step exposes an other region of said wafer to said reticle pattern features producing said varying overlay conditions, wherein said optimum photolithography process window takes into account regionality effects of the single wafer.